This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A data processing device which includes a circuit which consists of various circuit sections which can be fed with a supply voltage via a configuration of conductors, and

includes data processing means which constitute such a circuit section that can be fed with the supply voltage and are arranged to process data while utilizing a characteristic value, and also includes sequencing means which also constitute such a circuit section that can be fed with the supply voltage and are arranged to execute an algorithm in order to control the data processing means in conformity with this algorithm, which algorithm comprises a given number N of sub-algorithms which contain identical sequences of algorithm steps and can be executed in a given order each time when the algorithm is executed, and

wherein, upon processing of data by means of the data processing means under the control of the sequencing means in conformity with the algorithm, the data processing causes a current peak pattern to occur at the area of the configuration of conductors, the pattern configuration of the current peak pattern being dependent on the algorithm steps, on the processed data and on the characteristic value,

characterized in that the circuit additionally includes order fixation means which co-operate with the sequencing means and whereby, upon each execution of the algorithm, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms.

2. (previously presented) A data processing device as claimed in Claim 1, characterized in that the order fixation means include a random number generator, and

that, by means of the order fixation means upon each execution of the algorithm, an order for the execution of the N sub-algorithms is fixed, said order being defined by a random number generated by the random number generator.

3. (previously presented) A data processing device as claimed in Claim 2, characterized in that the order fixation means additionally include order selection means which contain feasible orders for the execution of the N sub-algorithms and co-operate with the random number generator, and that the order selection means can select an order from the feasible orders in conformity with a random number received from the random number generator.

4. (previously presented) A data processing device as claimed in Claim 1, characterized in that there are provided storage means which co-operate with the sequencing means and in which the algorithm is stored in the form of a program which contains N program blocks as sub-algorithms containing program instructions as algorithm steps.

5. (previously presented) A data processing device as claimed in Claim 1, characterized in that there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

6. (previously presented) A data processing device as claimed in Claim 1, characterized in that the data processing means are formed by means for the encryption and/or decryption of data.

7. (previously presented) A data processing device as claimed in Claim 1, characterized in that the data processing device is formed by a data carrier whose circuit is constructed in integrated technology.

8. (previously presented) A circuit for a data processing device which circuit consists of various circuit sections which can be fed with a supply voltage via a configuration of conductors, and

which circuit includes data processing means which constitute such a circuit section that can be fed with the supply voltage and are arranged to process data while utilizing a characteristic value, and also includes sequencing means which also constitute such a circuit section that can be fed with the supply voltage and are arranged to execute an algorithm in order to control the data processing means in conformity with this algorithm, which algorithm comprises a given number N of sub-algorithms which contain identical sequences of algorithm steps and can be executed in a given order each time when the algorithm is executed, and wherein, upon processing of data by means of the data processing means under the control of the sequencing means in conformity with the algorithm, the data processing causes a current peak pattern to occur at the area of the configuration of conductors, the pattern configuration of the current peak pattern being dependent on the algorithm steps on the processed data and on the characteristic value, characterized in that the circuit additionally includes order fixation means which co-operate with the sequencing means and whereby, upon each execution of the algorithm, an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms.

9. (previously presented) A circuit as claimed in Claim 8, characterized in that the order fixation means include a random number generator, and

that by means of the order fixation means upon each execution of the algorithm, an order for the execution of the N sub-algorithms random number generated by the random number generator.

10. (previously presented) A circuit as claimed in Claim 9, characterized in that the order fixation means additionally include order selection means which contain feasible orders for the execution of the N sub-algorithms and co-operate with the random number generator, and that the order selection means can select an order from the feasible orders in conformity with a random number received from the random number generator.

11. (previously presented) A circuit as claimed in Claim 8, characterized in that there are provided storage means which co-operate with the sequencing means and in which the algorithm is stored in the form of a program which contains N program blocks as sub-algorithms containing instructions as algorithm steps.

12. (previously presented) A circuit as claimed in Claim 8, characterized in that there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

13. (previously presented) A circuit as claimed in Claim 8, characterized in that the data processing means are formed by means for the encryption and/or decryption of data.

14. (previously presented) A circuit as claimed in Claim 8, characterized in that the circuit is intended for a data processing device which is formed by a data carrier, and that the circuit is constructed in integrated technology.